

SN65HVD147x 3.3-V Full-Duplex RS-485 Transceivers With ± 16 -kV IEC ESD

1 Features

- 1/8 Unit-Load Options Available
 - Up to 256 Nodes on the Bus
- Bus I/O Protection
 - $> \pm 30$ kV HBM protection
 - $> \pm 16$ kV IEC61000-4-2 Contact Discharge
 - $> \pm 4$ kV IEC61000-4-4 Fast Transient Burst
- Extended Industrial Temperature Range: -40°C to 125°C
- Large Receiver Hysteresis (70 mV) for Noise Rejection
- Low Power Consumption
 - < 1.1 mA Quiescent Current During Operation
 - Low Standby Supply Current: 10 nA Typical, < 5 μA (maximum)
- Glitch-Free Power-Up and Power-Down Protection for Hot-Plugging Applications
- 5-V Tolerant Logic Inputs Compatible With 3.3-V or 5-V Controllers
- Signaling Rate Options Optimized for: 500 kbps, 20 Mbps, 50 Mbps

2 Applications

- Industrial Automation
- Encoders and Decoders
- Building Automation
- Security and Surveillance Networks
- Telecommunications

3 Description

The SN65HVD147x family of full-duplex transceivers feature the highest ESD protection in the RS-485 portfolio, supporting ± 16 kV IEC61000-4-2 contact discharge and $> \pm 30$ kV HBM ESD protection. These RS-485 transceivers have robust 3.3-V drivers and receivers and are offered in a standard SOIC package as well as in a small-footprint MSOP package. The large receiver hysteresis of the SN65HVD147x devices provides immunity to conducted differential noise and the wide operating temperature enables reliability in harsh operating environments.

These devices each combine a differential driver and a differential receiver, which operate from a single 3.3-V power supply. Each driver and receiver has separate input and output pins for full-duplex bus communication designs. These devices all feature a wide common-mode voltage range which makes the devices suitable for multi-point applications over long cable runs.

The SN65HVD1471, SN65HVD1474, and SN65HVD1477 devices are fully enabled with no external enabling pins.

The SN65HVD1470, SN65HVD1473, and SN65HVD1476 devices have active-high driver enables and active-low receiver enables. A low, less than 5- μA standby current can be achieved by disabling both the driver and receiver.

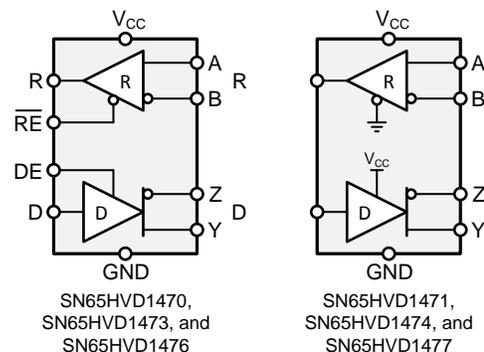
These devices are characterized from -40°C to 125°C .

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65HVD1471 SN65HVD1474 SN65HVD1477	MSOP (8) SOIC (8)	3.00 mm x 3.00 mm 4.90 mm x 3.91 mm
SN65HVD1470 SN65HVD1473 SN65HVD1476	MSOP (10) SOIC (14)	3.00 mm x 3.00 mm 8.65 mm x 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Block Diagram



4 Device and Documentation Support

4.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN65HVD1470	Click here				
SN65HVD1471	Click here				
SN65HVD1473	Click here				
SN65HVD1474	Click here				
SN65HVD1476	Click here				
SN65HVD1477	Click here				

4.2 Trademarks

All trademarks are the property of their respective owners.

4.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

4.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

5 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD1470D	PREVIEW	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HVD1470	
SN65HVD1470DGS	PREVIEW	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1470	
SN65HVD1470DGSR	PREVIEW	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1470	
SN65HVD1470DR	PREVIEW	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HVD1470	
SN65HVD1471D	PREVIEW	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1471	
SN65HVD1471DGK	PREVIEW	VSSOP	DGK	8	80	TBD	Call TI	Call TI	-40 to 125	1471	
SN65HVD1471DGKR	PREVIEW	VSSOP	DGK	8	2500	TBD	Call TI	Call TI	-40 to 125		
SN65HVD1471DR	PREVIEW	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1471	
SN65HVD1473D	PREVIEW	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HVD1473	
SN65HVD1473DGS	PREVIEW	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1473	
SN65HVD1473DGSR	PREVIEW	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1473	
SN65HVD1473DR	PREVIEW	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HVD1473	
SN65HVD1474D	PREVIEW	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1474	
SN65HVD1474DGK	PREVIEW	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1474	
SN65HVD1474DGKR	PREVIEW	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1474	
SN65HVD1474DR	PREVIEW	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1474	
SN65HVD1476D	PREVIEW	SOIC	D	14	50	TBD	Call TI	Call TI	-40 to 125	HVD1476	
SN65HVD1476DGS	PREVIEW	VSSOP	DGS	10	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1476	

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD1476DGSR	PREVIEW	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1476	
SN65HVD1476DR	PREVIEW	SOIC	D	14	2500	TBD	Call TI	Call TI	-40 to 125	HVD1476	
SN65HVD1477D	PREVIEW	SOIC	D	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1477	
SN65HVD1477DGK	PREVIEW	VSSOP	DGK	8	80	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1477	
SN65HVD1477DGKR	PREVIEW	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	1477	
SN65HVD1477DR	PREVIEW	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	VD1477	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

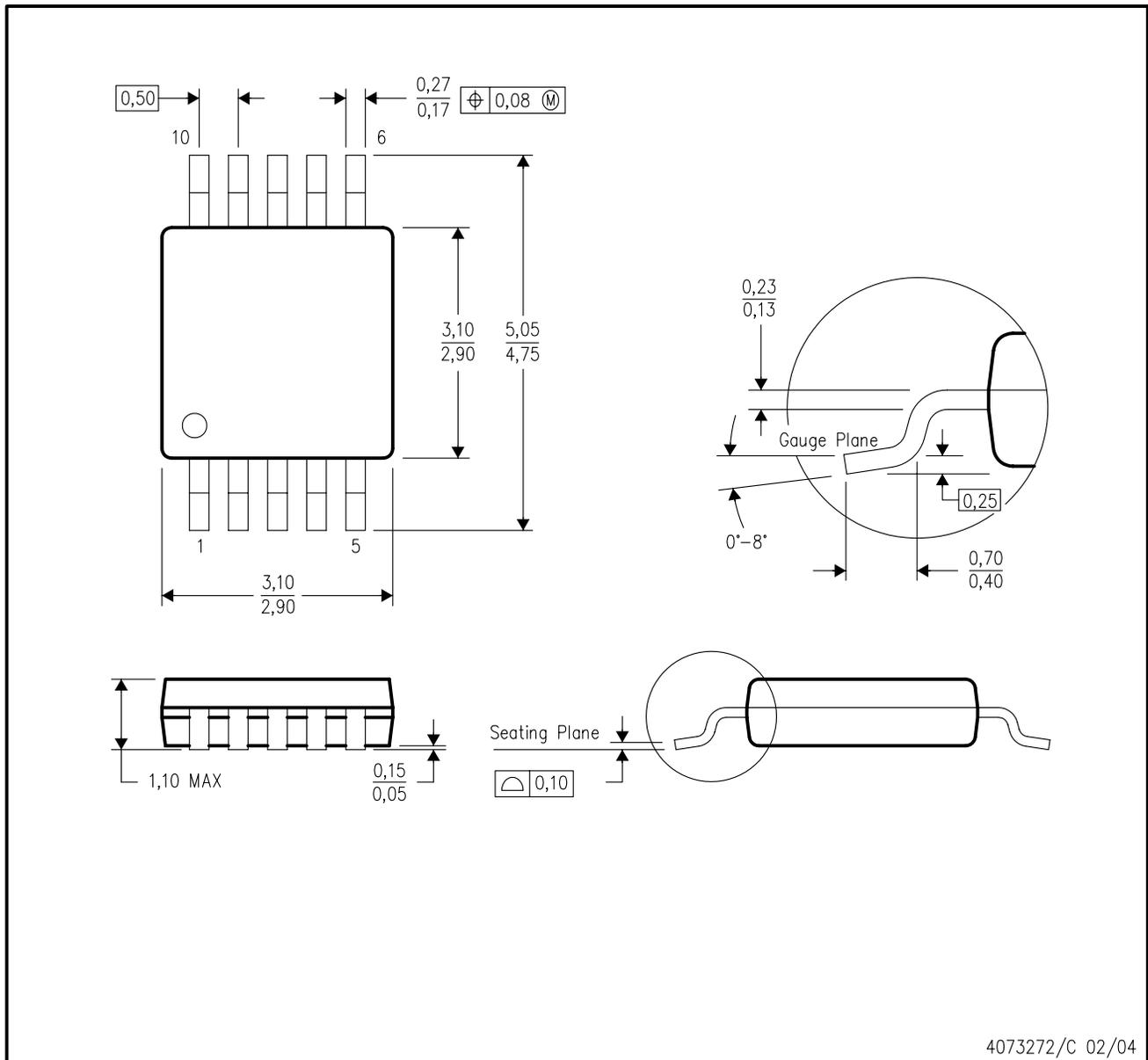
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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DGS (S-PDSO-G10)

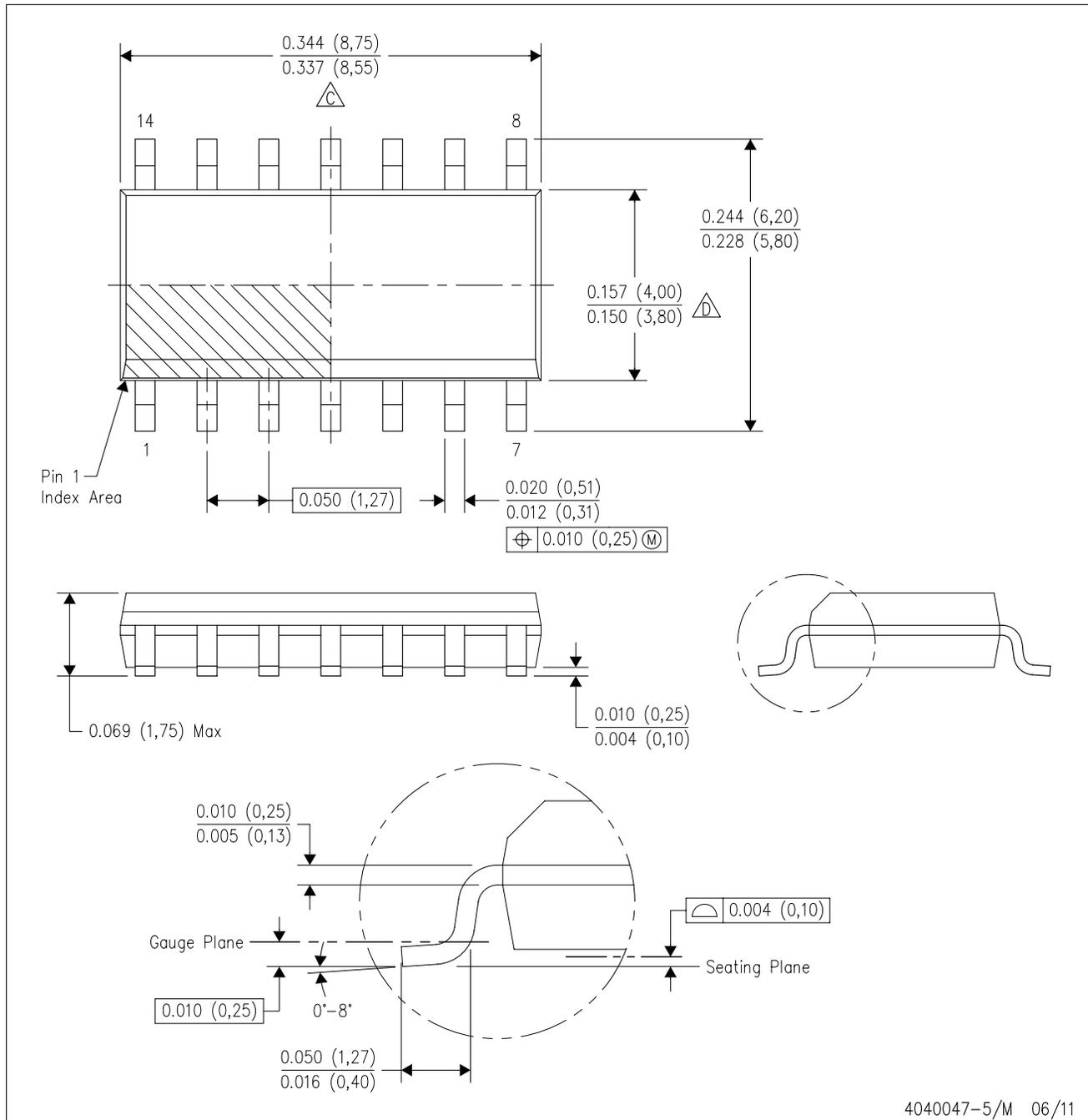
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 - D. Falls within JEDEC MO-187 variation BA.

D (R-PDSO-G14)

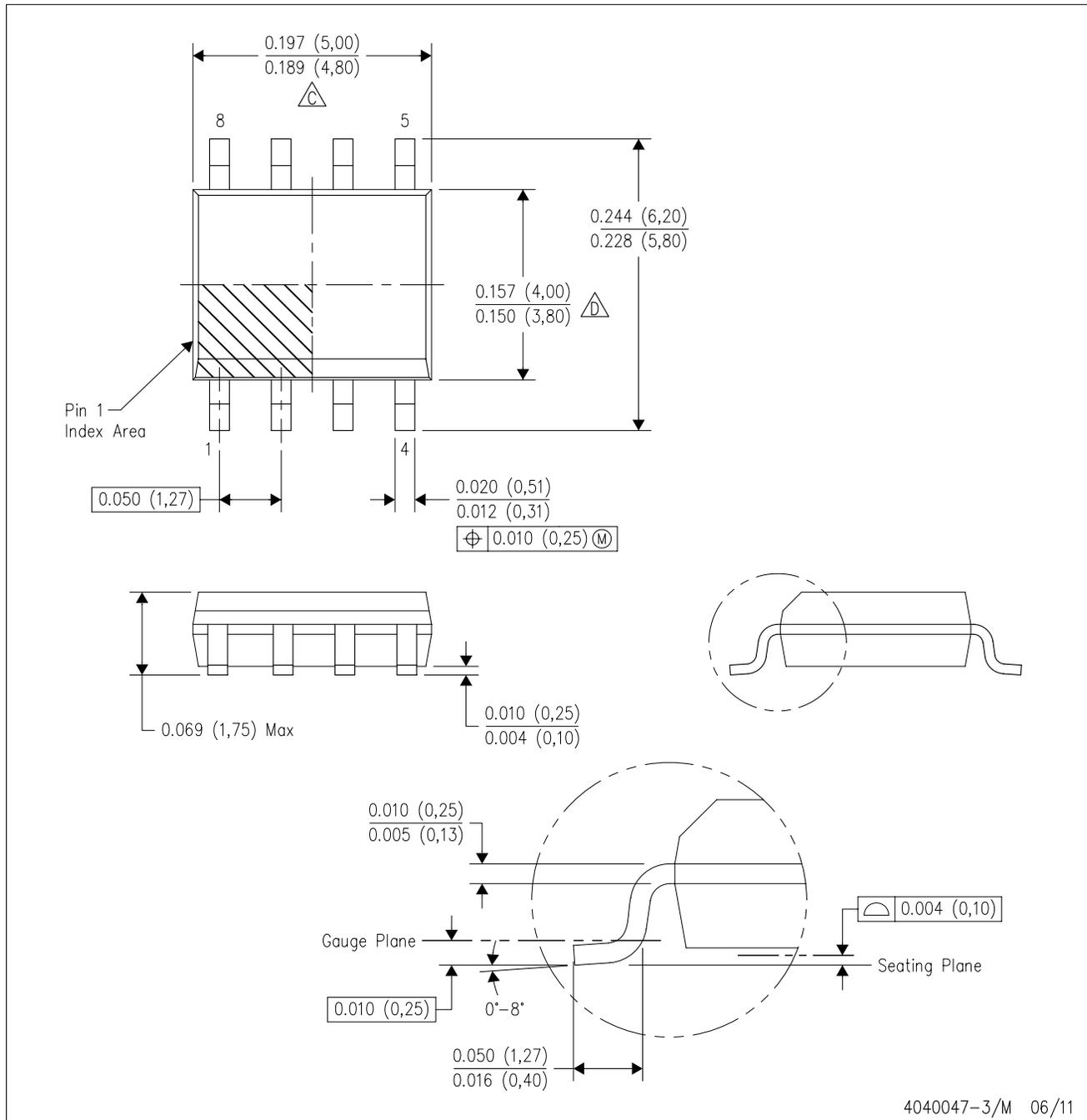
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4040047-3/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

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